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IEEE Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits

IEEE Computer Society

Developed by the
Test Technology Standards Committee

IEEE 1838™-2019

IEEE

STANDARDS

IEEE Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits

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Test Technology Standards Committee
of the
IEEE Computer Society

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Abstract: IEEE Std 1838 is a die-centric standard; it applies to a die that is intended to be part of a multi-die stack. This standard defines die-level features that, when compliant dies are brought together in a stack, comprise a stack-level architecture that enables transportation of control and data signals for the test of (1) intra-die circuitry and (2) inter-die interconnects in both (a) pre-stacking and (b) post-stacking situations, the latter for both partial and complete stacks in both pre-packaging, post-packaging, and board-level situations. The primary focus of inter-die interconnect technology addressed by this standard is through-silicon vias (TSVs); however, this does not preclude its use with other interconnect technologies such as wire-bonding.

Keywords: 3D test access, flexible parallel port, FPP, IEEE 1838, multi-tower stack, primary test access port, scan, secondary test access port, test, through-silicon via, TSV

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Introduction

This introduction is not part of IEEE Std 1838-2019, IEEE Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits.

Advancements in interconnect, assembly, and packaging technology have lead to a wide range of multi-die stack architectures. These die stacks need to be tested before they can be shipped with acceptable quality levels to customers. Consequently, three-dimensional design-for test (3D-DfT) structures that provide test access between the external stack I/Os and the various dies and inter-die interconnect are needed. Test access is needed for manufacturing phases that include both partially assembled and complete stacks. This standard addresses these issues.

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